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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR: Ricky S. Amos, et al.)
EXAMINER: Alexander G. Ghyka)
SERIAL NO.: 10/605,261)
ART UNIT: 2812)
FILING DATE: September 18, 2003)
DATE: June 7, 2005)
FOR: PROCESS OPTIONS FOR FORMING SILICIDED METAL GATES FOR
ADVANCED CMOS DEVICES

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Responsive to the Office Action mailed May 27, 2005, and the restriction requirement made therein, applicants provisionally elect Group I, claims 1-19, drawn to a method for forming a CMOS device, for continued examination herein.

Applicants traverse the restriction requirement on the grounds that 35 U.S.C. § 121 authorizes restriction only when the claimed invention is "independent and distinct" (emphasis added). A search of the subject matter of Group I, claims 1-19, drawn to a method for forming a CMOS device would necessarily require a search of the subject matter of Group II, claim 20, drawn to a method for forming an interconnect *and* a dual metal replacement gate structure for connection of NFET and PFET gates of a CMOS device. Thus the method delineated in Group II is not directed to an independent and distinct matter.

Applicants respectfully submit that a search of the subject matter of Group I will necessarily cover a search of the subject matter of Group II.

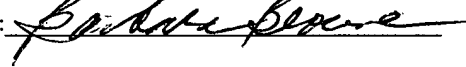
Respectfully submitted,


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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope addressed to: Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Name: Barbara Browne Date: June 7, 2005 Signature: 
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